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Amendments to the Specification:

Please replace the paragraph at page 6, line 26 through page 7, line 5 with the following amended paragraph:

Referring to FIG. 2, sequentially stacked first and second first insulating layer patterns 32 and first and second silicon layer patterns 34 are formed on the semiconductor 10, on which the upper surfaces of the collector region 16 and the collector sinker 18 are exposed, while exposing the collector region 16. To this end, a first insulating layer, for example, an oxide layer or a nitride layer, are formed on the semiconductor substrate 10, and a silicon layer is formed thereon. Here, the silicon layer can be formed of a silicon germanium (SiGe) layer. Thereafter, the silicon layer is dry etched by photolithography to form the first and second silicon layer patterns 34, and the first insulating layer is wet etched using the first and second silicon layer patterns 34 as an etch mask to form the first and second first insulating layer patterns 32. Here, the first insulating layer patterns 32 can be formed by dry etching instead of wet etching.

Please replace the paragraph at page 7, lines 6-14 with the following amended paragraph:

Referring to FIG. 3, a p+-type first base semiconductor layer 40 formed of a SiGe layer is formed on the resultant structure, in which the collector region 16 is exposed by the first and second silicon layer patterns 34, to a thickness of hundreds to 2,000 Å. Here, the first base semiconductor layer 40 is formed by a selective epitaxial growing method at a relatively low temperature, which is selected from a temperature range from 500 to 900℃. Therefore, the portion of the first base semiconductor layer 40 contacting the collector region 16 is formed of a mono-crystalline silicon layer, and a SiGe layer in which p-type impurities such as boron (B) are doped at a proper dosage and gradient, is formed on the mono-crystalline silicon layer.

Please replace the paragraph at page 8, lines 8-13 with the following amended paragraph:

Referring to FIG. 8, silicon is grown on the exposed surface of the first base semiconductor layer 40 by a selective epitaxial growing method, which is performed at a relatively low temperature selected from a range from 500 to 900℃, so that second base semiconductor layers 60, in a pattern of selectively epitaxially grown silicon, are formed to a thickness of about 1,000 Å. Here, the second base semiconductor layers 60 are formed to include p-type impurities. In this case, the silicon is epitaxially grown on the exposed surfaces of the emitter region 44a.

Please replace the paragraph at page 8, lines 14-22 with the following amended paragraph:

Referring to FIG. 9, unneeded portions of the first insulating layer patterns 32, the silicon layer patterns 34, the first base semiconductor layer 40, the third insulating layer 46, and the second base semiconductor layers 60 are removed by photolithography, and base ohmic layers 70 formed of metal silicide are formed on the second base semiconductor layers 60, the base ohmic layers 70 being a pattern of metal silicide. To this end, the exposed silicon of the second base semiconductor layers 60 is covered with metal, such as titanium or cobalt, and the metal is converted into metal silicide. Here, metal silicide layers are formed on the exposed silicon portions of the semiconductor substrate 10, i.e., the exposed surfaces of the emitter region 44a and the upper surface of the collector sinker 18.